REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
	--	Original Release	3/11/05	

REV STATUS	REV	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

REV STATUS	REV																
SHEETS	SHEET	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32

CONTRACT No.:

		DATE
DRAWN	J. McBride	3/17/05
CHECK		
APPD.	[signature]	3/18/05
ENGR.		
PROD.		
QC.	[signature]	3/18/05

American Microwave Corporation

7311-G Grove Road, Frederick, MD 21704

ACCEPTANCE TEST PROCEDURE

MODEL: SWN-RRA-2DR-LSI
OPTIONS: NG, DB
SINGLE POLE DOUBLE THROW PIN DIODE SWITCH

SIZE: A	FSCM: 60483	DRAWING No: 100-7382
REV: -	SCALE: N/A	SHEET 1 OF 14

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ACCEPTANCE

TEST PROCEDURE
(ATP)

FOR

AMC MODEL NUMBER: SWN-RRA-2DR-LSI
OPTIONS: NG, DB

SINGLE POLE DOUBLE THROW
PIN DIODE SWITCH

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1.0 SCOPE

The purpose of this document is to provide an electrical testing procedure for AMC Model SWN-RRA-2DR-LSI Options NG, DB Single Pole Double Throw PIN-Diode Switch. This procedure is only to be performed by a test technician experienced in the testing of RF and microwave devices.

2.0 EQUIPMENT LIST

The following equipment, or equivalent, are to be used in conjunction with this Acceptance Test Procedure (ATP) provided that all said equipments have displayed a valid calibration notice that can be traced to the National Institute of Standards and Technologies (NIST).

TABLE OF APPROVED TEST EQUIPMENT
TABLE I

Item Number	ITEM	MANUFACTURER	MODEL NUMBER
1	RF Source	Hewlett Packard	8350B
1a	RF Source, Plug-In	Hewlett Packard	83692A
2	Power Meter	Gigatronic	8541/8541C
2a	Power Sensor	Gigatronic	80401A
3	Power Supply (2 needed)	Agilent	3631A
4	Termination, 50 ohm (2 needed)	Mid-West	2444
5	Negative Diode Detector	AMC	LD-50-SHS-N-1
6	Vector Network Analyzer	Agilent Wiltron	8722D/8722ES/8720D 37347A
7	Function Generator	Hewlett Packard	3312A
8	Multimeter	Agilent	34401A
9	Calibrated Short/Open	Wiltron	22KF50
10	Pulse Generator	Hewlett Packard	8013B
11	Oscilloscope	Tektronix	TDS3054/TDS3014B
12	Spectrum Analyzer	Agilent	E4407B
13	Low Pass Filter	AMC	N/A

3.0 TEST CONDITIONS

3.1 Lot Acceptance Tests, paragraph 4.0, are design inherent and shall be performed on at least 1 unit at ambient temperature. In addition, at least one unit shall be tested at hot, cold, and ambient temperatures. See Table II for operating temperature data.

3.1.1 Results of these tests shall be recorded on the Lot Acceptance Test Data Sheet.

TABLE II

Operating Temperature	
COLD	-55° C
AMBIENT	+25° C
HOT	+85° C

3.2 Test paragraphs 5.0 and 6.0 shall be performed on all finished units prior to shipment.

3.2.1 All tests shall be performed at ambient temperature.

3.2.2 Results of these tests shall be recorded on the Acceptance Test Data Sheets

4.0 LOT ACCEPTANCE TESTS

4.1 ELECTRICAL INTERFACES

4.1.1 With equipment set up as shown in Figure I, apply 2 Volts to the control input and verify the UUT reaches Logic " 1" in accordance with Table III. Record the control voltage onto the test data sheet.

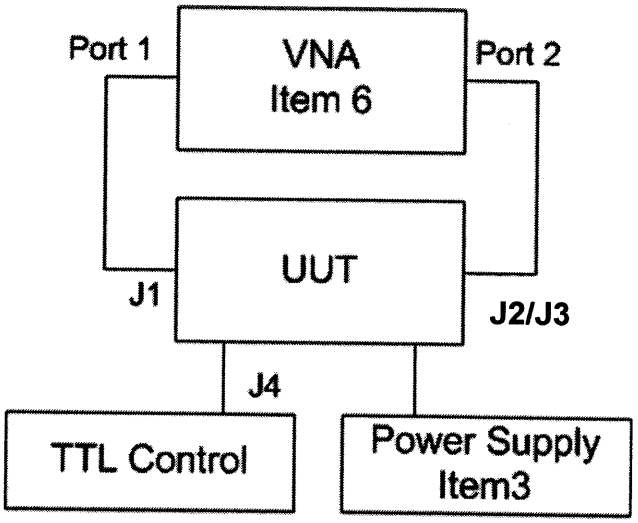

FIGURE I

Table III

Control Signal (J4)	Path On	Path Off
Logic " 0"	J1 – J2	J1 – J3
Logic " 1"	J1 – J3	J1 – J2

4.1.2 Apply 0.8 Volts to the control input and verify the UUT reaches Logic " 0" in accordance with Table III. Record the control voltage onto the test data sheet.

4.2 RESPONSE TIME

4.2.1 Measurement of switching speed characteristics.

4.2.1.1 Set up the equipment as shown in Figure II. Adjust the pulse width on the pulse generator to 1 μsec TTL "high" and 1 μsec TTL "low".

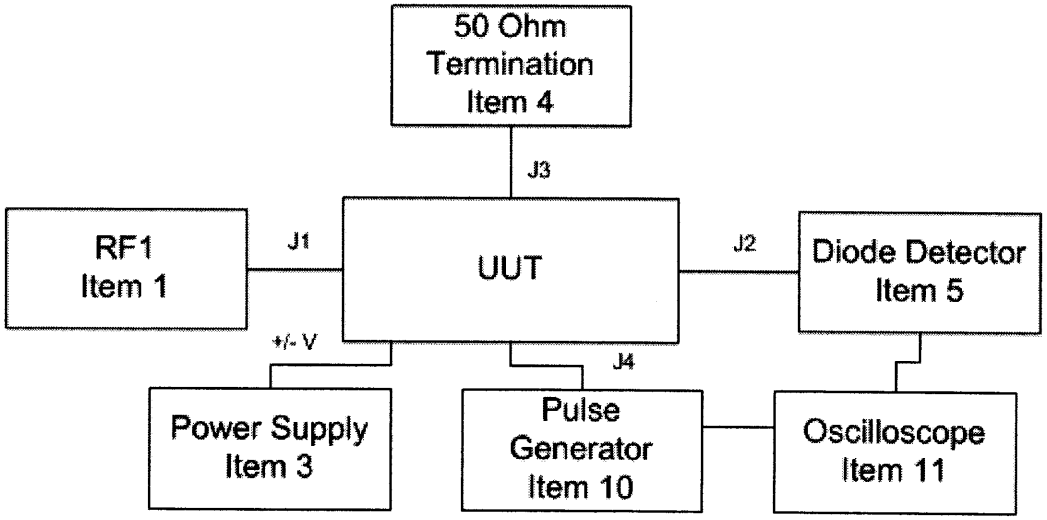

FIGURE II

4.2.1.2 Pulse from off to on position and vise versa by connecting the pulse generator to the control logic input of the selected RF port.

4.2.1.3 Delay time Measurement (Off to On)

4.2.1.3.1 Measure the output of the Detector ON-Time by observing the time delay between the 50% voltage point of the pulsed TTL input to within 1.0 dB of the low insertions loss state for the selected path. Record the ON-Time onto the Test Data Sheet.

4.2.1.3.2 Repeat for the J1 to J3 Path.

4.3 VIDEO SPIKE LEAKAGE

4.3.1 Setup equipment as shown in Figure III. Apply a TTL High to control input. Adjust pulse generator to obtain a 0 volt to + 3.3 volt square wave, 100 KHz repetition rate. Adjust oscilloscope to view transients with a minimum bandwidth of 300 MHz and record the peak transient voltage on the Test Data Sheet.

4.3.2 Repeat procedure for the J2 RF port.

4.3.3 Repeat procedure for the J3 RF port.

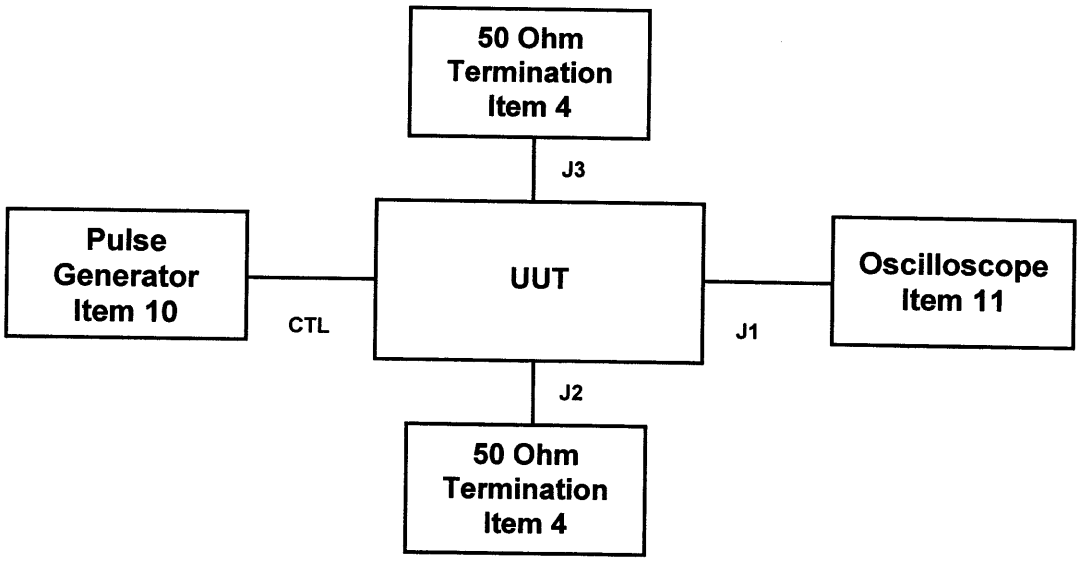

FIGURE III

4.4 SPECTRAL ACTIVITY

4.4.1 Setup equipment as shown in Figure IV. Apply a TTL High to control input. Adjust pulse generator to obtain a 0 volt to + 3.3 volt square wave, 100 KHz repetition rate. Observe the maximum value shown on the spectrum analyzer and record on the Test Data Sheet.

4.4.2 Repeat procedure for the J2 RF port.

4.4.3 Repeat procedure for the J3 RF port.

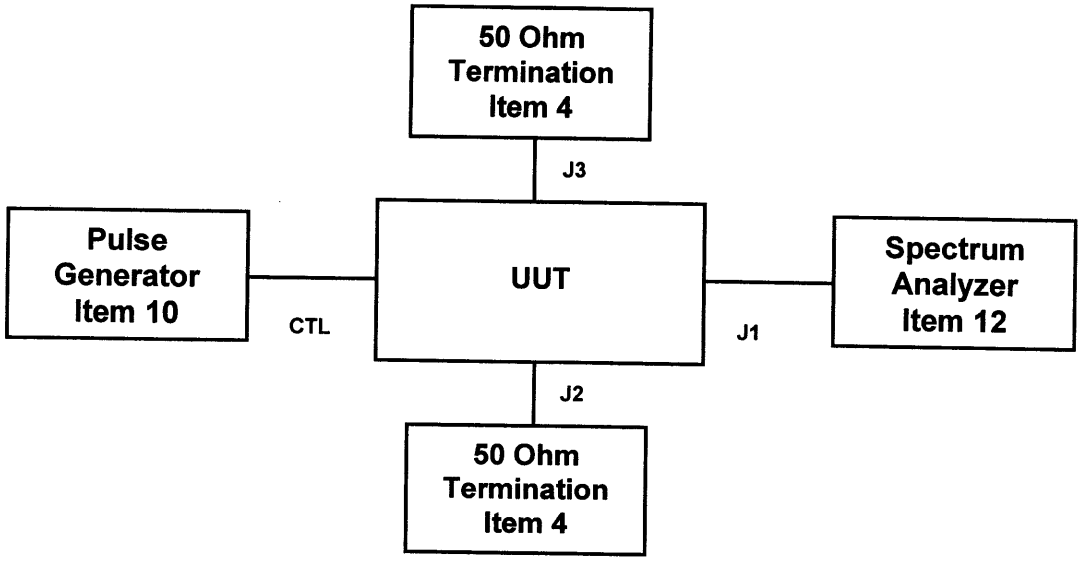

FIGURE IV

5.0 INPUT POWER REQUIREMENTS

5.1 With equipment set up as shown in Figure V, apply all logic combinations to the control input. Record the maximum current measured for the + 5 Vdc Line onto the test data sheet.

5.1.1 Repeat for the – 15 Vdc line.

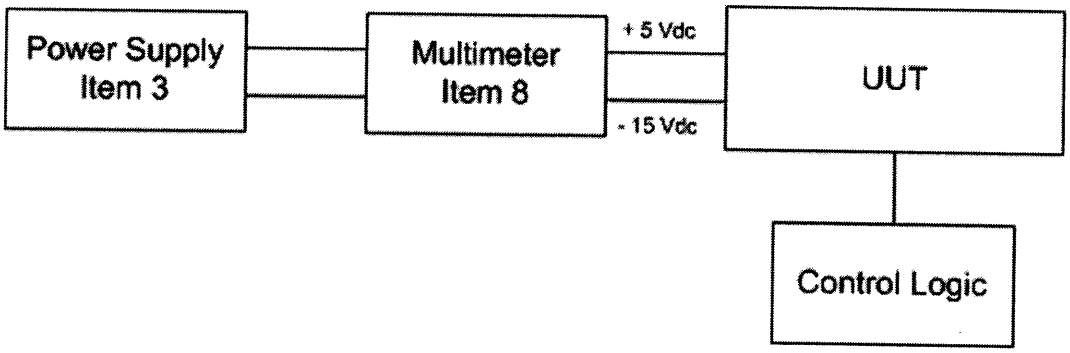

FIGURE V

6.0 INSERTION LOSS, VSWR, AND ISOLATION

6.1 Calibration of the Vector Network Analyzer (VNA). (For Insertion Loss, Isolation, and VSWR tests)

6.1.1 Connect the test equipment as in Figure VI. Set VNA with frequencies from 2.0 GHz to 18.0 GHz. Set RF power level to + 0 dBm. Connect the open on Port 1 and short to Port 2. Press Cal button, then select full 2 port Cal and follow VNA instructions.

6.1.2 Save calibration to the registry.

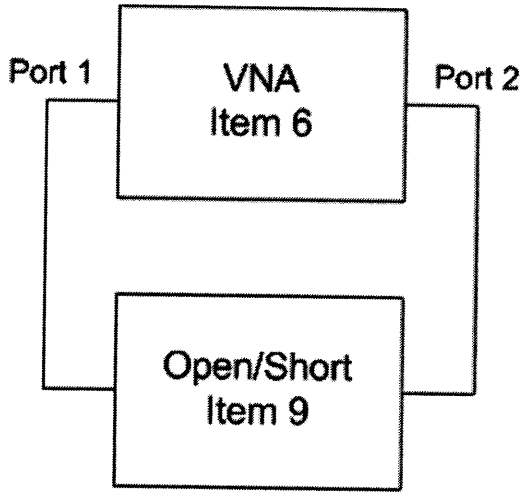

FIGURE VI

6.2 **Measurement of the Unit Under Test (UUT).**

6.2.1 **Connect the test equipment and the UUT as in Figure VII with common port (J1) as RF input and (J2) as RF output.**

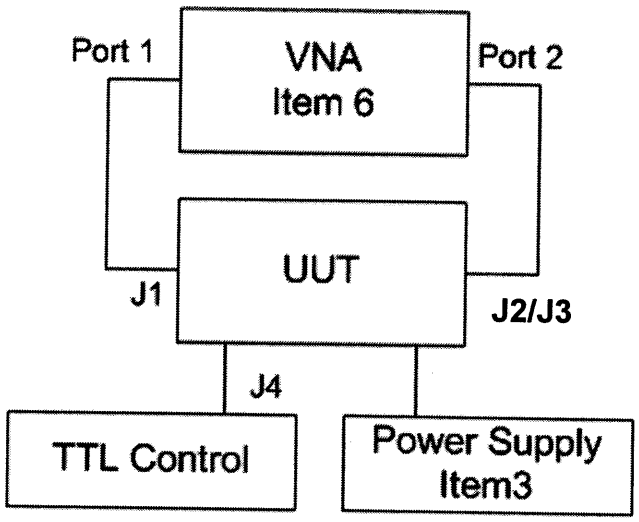

FIGURE VII

6.2.2 **Apply the TTL Logic Code to the UUT via the Table IV.**

Table IV

Control Signal (J4)	Path On	Path Off
Logic " 0"	J1 – J2	J1 – J3
Logic " 1"	J1 – J3	J1 – J2

6.2.3 **INSERTION LOSS/LOSS FLATNESS**

6.2.3.1 **Observe and record onto the Test Data Sheet the worst case insertion loss (S21) displayed on the VNA.**

6.2.3.2 **Observe and record onto the Test Data Sheet the insertion loss flatness for any 500MHz Band (S21) displayed on the VNA.**

6.2.3.3 **Repeat for the J1 to J3 Path.**

6.2.4 VSWR

6.2.4.1 Observe and record the worst case input (S11) VSWR, displayed on the VNA, onto the Test Data Sheet for the J1 to J2 path,

6.2.4.2 Repeat for the J1 to J3 path.

6.2.5 ISOLATION

6.2.5.1 Set VNA to observe S21, press display to memory then press data/memory button to calibrate out the insertion loss.

6.2.5.2 Apply proper logic to the UUT to have no RF thru path J1 to J2.

6.2.5.3 Observe and record onto the test data sheet the worst case isolation displayed on the VNA.

6.2.5.4 Repeat for the J1 to J3 path.

Model No: SWN-RRA-2DR-LSI
Options: NG, DB
Acceptance Test Data Sheet 1 of 1

JOB: _____ CUSTOMER: _____

S/N: _____ TESTED BY: _____ DATE: _____

QA APPROVAL: _____ DATE: _____

Para.	Parameter	Requirement	Tolerance	Measured Value	Pass/Fail
5.0	Input Power Requirements				
	- 15.5 Vdc	-15 VDC ± 1.56 VDC	75 mA Max.	mA	
	+ 5 VDC	+5 VDC +0.2VDC/-0.3VDC	150 mA Max.	mA	
6.2.3.1	Insertion Loss				
	J1-J2	3.5 dB (2.0 to 18.0 GHz)	Max.	dB	
	J1-J3	3.5 dB (2.0 to 18.0 GHz)	Max.	dB	
6.2.3.2	Insertion Loss Flatness				
	J1-J2	±1.5 dB in any 500 MHz Band	±1.5 dB	± dB	
	J1-J3	±1.5 dB in any 500 MHz Band	±1.5 dB	± dB	
6.2.4	Input VSWR (Ref to 50 Ohms)				
	J1-J2	2.0:1	Max.	dB	
	J1-J3	2.0:1	Max.	dB	
6.2.5	Isolation				
	J1-J2	60 dB (2.0 to 18.0 GHz)	Min.	dB	
	J1-J3	60 dB (2.0 to 18.0 GHz)	Min.	dB	

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Model No: SWN-RRA-2DR-LSI
Options: NG, DB
Lot Acceptance Test Data Sheet 1 of 1

JOB: _____ CUSTOMER: _____

S/N: _____ TESTED BY: _____ DATE: _____

TEMP: _____ QA APPROVAL: _____ DATE: _____

Para.	Parameter	Requirement	Tolerance	Measured Value	Pass/Fail
4.1	Electrical Interfaces				
		Logic 0 J1 to J2 IL mode and J1 to J3 Isolation Mode	-0.5 to 0.8 Volts	Vdc	
		Logic 1 J1 to J3 IL mode and J1 to J2 Isolation Mode	2.0 to 3.5 Volts	Vdc	
4.2	Response Time				
	J1-J2	350 nSec (from 50% point of leading edge of control input to within 1.0 dB of the low insertions loss state for the selected path)	Max.	nS	
	J1-J3	350 nSec (from 50% point of leading edge of control input to within 1.0 dB of the low insertions loss state for the selected path)	Max.	nS	
4.3	Video Spike Leakage				
	J1	150 mV Peak @ 300 Mhz bandwidth	Max	mV p	
	J2	150 mV Peak @ 300 Mhz bandwidth	Max	mV p	
	J3	150 mV Peak @ 300 Mhz bandwidth	Max	mV p	
4.4	Spectral Activity				
	J1	-70 dBm Maximum 2 to 18 GHz	Max	dBm	
	J2	-70 dBm Maximum 2 to 18 GHz	Max	dBm	
	J3	-70 dBm Maximum 2 to 18 GHz	Max	dBm	

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