REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
	--	Original Release	6/24/05	
	--	Modified	1/20/06	

REV STATUS	REV	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

REV STATUS	REV																
SHEETS	SHEET	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32

CONTRACT No.:			American Microwave Corporation 7311-G Grove Road, Frederick, MD 21704		
		DATE			
DRAWN	J. McBride	6/24/05			
CHECK	Y. Rong	1/20/06	ACCEPTANCE TEST PROCEDURE MODEL: MSN-4DT-561R875 OPTIONS: NG SINGLE POLE FOUR THROW PIN DIODE SWITCH		
APPD.					
ENGR.					
PROD.					
QC.					
			SIZE: A	FSCM: 60483	DRAWING No: 100-7461
			REV: -	SCALE: N/A	SHEET 1 OF 14

American Microwave Corporation, 7311-G Grove Road, Frederick, MD 21704
Telephone: 301-662-4700 ● Fax: 301-662-4938 ● Email: sales@americanmicrowavecorp.com

ACCEPTANCE

TEST PROCEDURE
(ATP)

FOR

AMC MODEL NUMBER: MSN-4DT-561R875
OPTIONS: NG

SINGLE POLE FOUR THROW
PIN DIODE SWITCH

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TABLE OF CONTENTS

1.0 SCOPE

The purpose of this document is to provide an electrical testing procedure for AMC Model MSN-4DT-561R875 Options NG Single Pole Four Throw PIN-Diode Switch. This procedure is only to be performed by a test technician experienced in the testing of RF and microwave devices.

2.0 EQUIPMENT LIST

The following equipment, or equivalent, are to be used in conjunction with this Acceptance Test Procedure (ATP) provided that all said equipments have displayed a valid calibration notice that can be traced to the National Institute of Standards and Technologies (NIST).

TABLE OF APPROVED TEST EQUIPMENT
TABLE I

Item Number	ITEM	MANUFACTURER	MODEL NUMBER
1	RF Source	Hewlett Packard	8350B
1a	RF Source, Plug-In	Hewlett Packard	83692A
2	Power Meter	Gigatronic	8541/8541C
2a	Power Sensor	Gigatronic	80401A
3	Power Supply (2 needed)	Agilent	3631A
4	Termination, 50 ohm (2 needed)	Mid-West	2444
5	Negative Diode Detector	AMC	LD-50-SHS-N-1
6	Vector Network Analyzer	Agilent Wiltron	8722D/8722ES/8720D 37347A
7	Function Generator	Hewlett Packard	3312A
8	Multimeter	Agilent	34401A
9	Calibrated Short/Open	Wiltron	22KF50
10	Pulse Generator	Hewlett Packard	8013B
11	Oscilloscope	Tektronix	TDS3054/TDS3014B
12	Spectrum Analyzer	Agilent	E4407B
13	Low Pass Filter	AMC	N/A
14	Noise Figure Meter	Hewlett Packard	8970B
15	Directional Coupler	Krytar	101020010
16	Amplifier	Mini Circuit	ZHL-42/SMA

3.0 TEST CONDITIONS

3.1 Lot Acceptance Tests, paragraph 4.0, shall be performed on the first two production units only.

3.1.1 All tests shall be performed at ambient temperature unless otherwise noted.

3.1.2 Results of these tests shall be recorded on the Lot Acceptance Test Data Sheet.

3.2 Test paragraph 5.0 and 6.0 shall be performed on all finished units prior to shipment.

3.2.1 All tests shall be performed at ambient temperature unless otherwise noted. See Table II for operating temperature data.

3.2.2 Results of these tests shall be recorded on the Acceptance Test Data Sheet.

TABLE II

Operating Temperature	
COLD	**-40º C (+0º C/-3º C)**
AMBIENT	**+25º C (± 3º C)**
HOT	**+85º C (+3º C/-0º C)**

4.0 LOT ACCEPTANCE TESTS

4.1 SWITCHING TIME

4.1.1 Measurement of switching speed characteristics.

4.1.1.1 Set up the equipment as shown in Figure I. Adjust the pulse width on the pulse generator to 1 μsec TTL "high" and 1 μsec TTL "low".

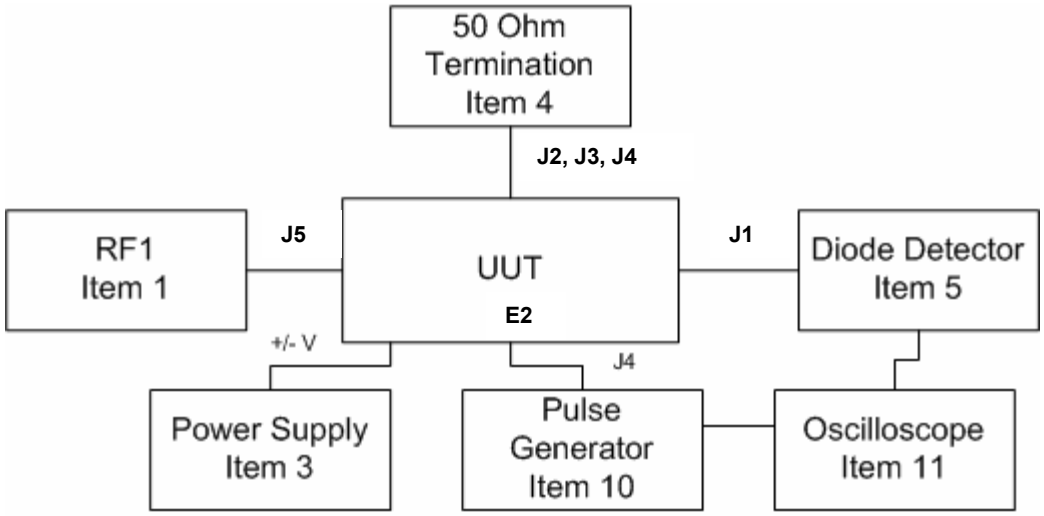

FIGURE I

4.1.1.2 Configure the pulse generator to generate a required pulse.

4.1.1.3 Connecting the pulse generator's output to the control logic input of the selected RF port.

4.1.1.4 Switching time (Off to On, On to Off)

4.1.1.4.1 Measure the output of the Detector from the 50% point on the leading edge of the TTL control pulse to the 90% amplitude on the leading edge of the RF output waveform. Record the switching time onto the Test Data Sheet.

4.1.1.4.2 Repeat all cases.

4.1.1.5 Rise/Fall Time

4.1.1.5.1 Rise Time 10% to 90%

4.1.1.5.1.1 Measure the output of the Detector from the 10% point on the leading edge of the TTL control pulse to the 90% point on the leading edge of the TTL control pulse. Record the rise time onto the Test Data Sheet.

4.1.1.5.2 Fall Time 90% to 10%

4.1.1.5.2.1 Measure the output of the Detector from the 90% point on the leading edge of the TTL control pulse to the 10% point on the leading edge of the TTL control pulse. Record the fall time onto the Test Data Sheet.

4.2 VIDEO FEEDTHROUGH*

4.2.1 Set up the equipment as shown in Figure II. Adjust the pulse width on the pulse generator to 1 μsec TTL "high" and 1 μsec TTL "low".

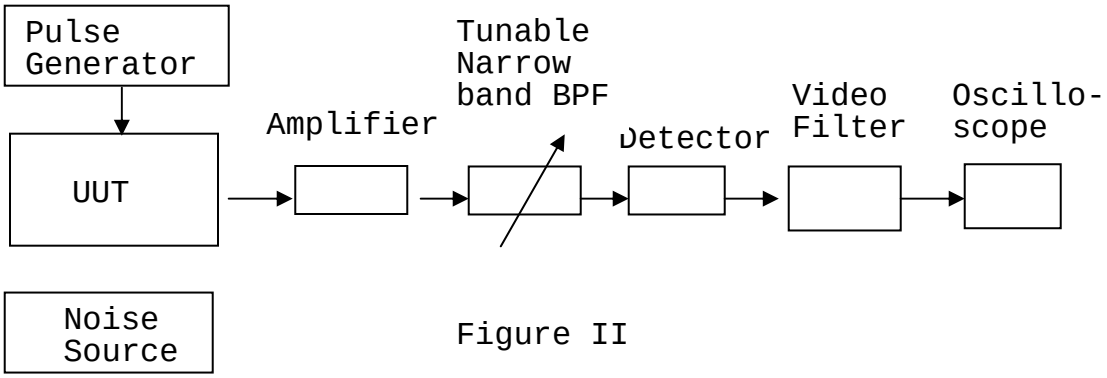

Figure II

4.2.2 Calibrate the test setup

a. In Figure II, a calibrated noise source should be as the input source.

b. Tune the narrow band tunable filter to cover the sub-frequency band from Freq1 to Freq 2.

c. Configure the signal source so that it will produce the known noise signals from Freq 1 to Freq 2.

d. Adjust the input noise source power and record the data from the Oscilloscope and repeat this procedure till all the power levels are covered.

e. Repeat Steps b, c, and d till the frequency band of interest is covered.

4.2.3 In Figure II, UUT should be as the input source. Except the port to be tested, all the ports in UUT should be connected to 50 ohms loads. The port to be tested should be used as the input port for the following stage as shown in Figure II. For the control pins, 2 complementary TTL control signals should be applied to the corresponding control pins and "HIGH" should be applied to the remaining two control pins.

4.2.4 Tune the narrow band tunable filter from Freq 1 to Freq 2, record the data from the oscilloscope. Repeat this process till all the frequency band of interest is covered.

4.2.5 Compute the video transient level based on the recorded data from 4.22 and 4.2.4.

4.2.6 Repeat the above procedures till all the ports are tested.

*** This test approach measures the power level of the video signals in frequency domain only.**

4.3 POWER SUPPLY

4.4 RESPONSE TIME

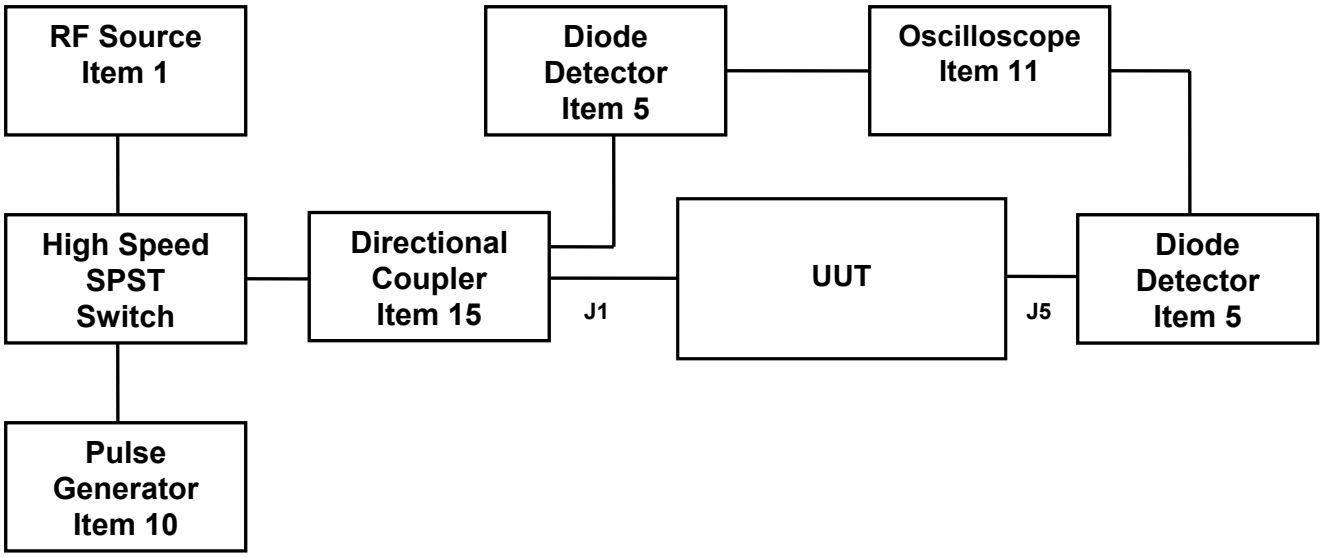

FIGURE III

5.0 ACCEPTANCE TESTS

5.1 FREQUENCY

5.1.1 **If the switch does not function over the full frequency range in any of the following tests the unit does not meet the frequency requirement. If all tests are met record the full frequency range on the Test Data Sheet.**

5.2 SELECTED PATH GAIN (RETURN LOSS)

5.2.1 **Refer to section 6.0.**

5.3 GAIN DEVIATION

5.3.1 **The gain deviation is calculated by finding the difference between each selected path gain measured in 6.2.3. The largest deviation shall be recorded on the Test Data Sheet.**

5.4 NOISE FIGURE

5.4.1 **Calibrate Noise Figure Meter.**
5.4.2 **Set up the equipment as shown in Figure IV. Set the VNA to output +5dBm CW.**

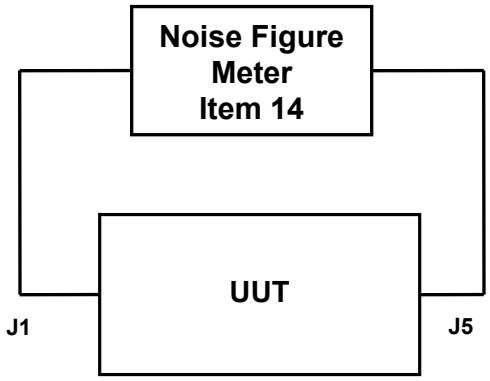

FIGURE IV

5.4.3 **Observe and record onto the Test Data Sheet the noise figure displayed on the Noise Figure Meter.**

5.4.4 **Repeat for path J2 to J5.**

5.4.5 **Repeat for path J3 to J5.**

5.4.6 **Repeat for path J4 to J5.**

5.5 MAXIMUM RF INPUT SIGNAL

5.5.1 Set up the equipment as shown in Figure V. Set the output of the Amplifier to +25dBm CW.

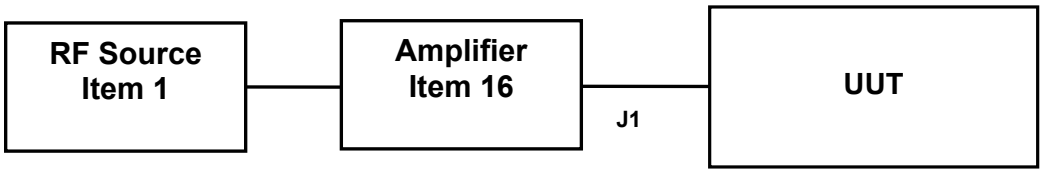

FIGURE V

5.5.2 If the UUT does not suffer any damage or permanent degradation then record PASS on the Test Data Sheet.

5.5.3 Set the Pulse Generator to a 1uS pulse and 0.1% duty cycle. If the unit is reading Return Loss in accordance with section 6.0 then record PASS on the Test Data Sheet.

5.5.4 Repeat for path J2 to J5.

5.5.5 Repeat for path J3 to J5.

5.5.6 Repeat for path J4 to J5.

5.6 INPUT 1dB COMPRESSION POINT

5.6.1 Set up the equipment as shown in Figure VI.

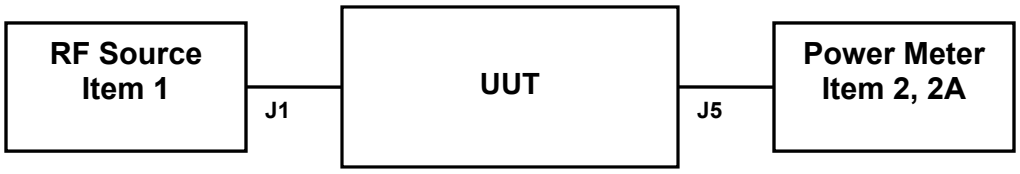

FIGURE VI

5.6.2 Vary the source from +1 dBm to +10 dBm and measure the output power level of the UUT.

5.6.3 Record where the output level compresses by 1dBm on the Test Data Sheet.

5.6.4 Repeat for path J2 to J5.

5.6.5 Repeat for path J3 to J5.

5.6.6 Repeat for path J4 to J5.

5.7 HARMONICS AND SPURRIOUS SIGNALS

5.7.1.1 HARMONICS

5.7.1.1.1 Setup equipment as shown in Figure VII. Pulse J1 according to Table III. Adjust pulse generator to obtain a 0 volt to +3.3 volt square wave, 100 KHz repetition rate. Set the source to 5dBm CW. Observe the maximum harmonic value shown on the spectrum analyzer and record on the Test Data Sheet.

5.7.1.2 SPURIOUS SIGNALS

5.7.1.2.1 Setup equipment as shown in Figure VII. Pulse J1 according to Table III. Adjust pulse generator to obtain a 0 volt to +3.3 volt square wave, 100 KHz repetition rate. Set the source to 5dBm CW. Observe the maximum spurious signal value shown on the spectrum analyzer and record on the Test Data Sheet.

5.7.2 Repeat procedure for the J2 RF port.

5.7.3 Repeat procedure for the J3 RF port.

5.7.4 Repeat procedure for the J4 RF port.

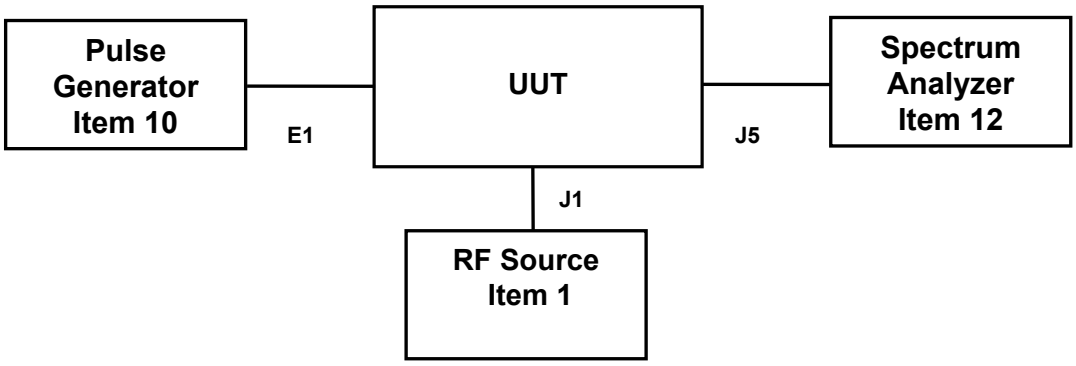

FIGURE VII

5.8 RF ISOLATION

5.8.1 Refer to section 6.0.

5.9 INSERTION PHASE VARIATION

5.9.1 Refer to section 6.0 to set the VNA up for Insertion Loss. Set the VNA to measure Phase.

5.9.2 Use Program "Read From VNA 2.4.vee" to capture phase variation plot and data. Record phase variation in the Test Data Sheet.

5.9.3 Repeat for path J2 to J5.

5.9.4 Repeat for path J3 to J5.

5.9.5 Repeat for path J4 to J5.

5.10 INSERTION GAIN VARIATION

5.10.1 Refer to section 6.0 to set the VNA up for Insertion Loss.

5.10.2 Use Program "Read From VNA 2.4.vee" to capture gain variation plot and data. Record gain variation in the Test Data Sheet.

5.10.3 Repeat for path J2 to J5.

5.10.4 Repeat for path J3 to J5.

5.10.5 Repeat for path J4 to J5.

5.11 INPUT AND OUTPUT VSWR

5.11.1 Refer to section 6.0.

5.12 SWITCH CONTROL CHARACTERISTICS

5.12.1 With equipment set up as shown in Figure VII, apply 2.4 Volts to the control input and verify the UUT reaches Logic "1" for each Logic combination called out in 5.13. Record the control voltage onto the test data sheet.

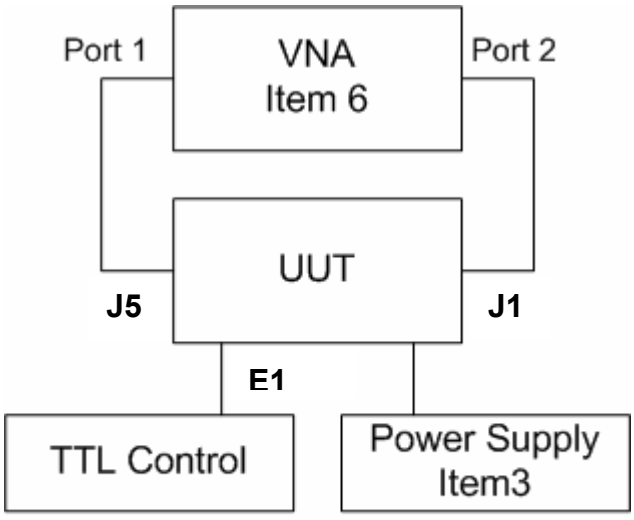

FIGURE VII

5.12.2 Apply 0.8 Volts to the control input and verify the UUT reaches Logic "0" for each Logic combination called out in 5.13. Record the control voltage onto the test data sheet

5.13 CONTROL LINES

5.13.1 The control lines shown in Table III shall be used to control the input ports of the switch.

Table III

Control/ Word Lines				Selected Path
E4	E3	E2	E1	
1	1	1	0	J1 – J5
1	1	0	1	J2 – J5
1	0	1	1	J3 – J5
0	1	1	1	J4 – J5

5.13.2 Each Control input combination shall be tested according to 5.12 and recorded in the Test Data Sheet.

5.14 DC BLOCK

5.14.1 With the UUT powered up check with a multi-meter RF ports J1 thru J5 for DC current. If no current is detected record PASS on the Test Data Sheet.

5.15 DC POWER REQUIREMNETS

5.15.1 With equipment set up as shown in Figure VIII, apply all logic combinations to the control input. Record the maximum current measured for the + 5 Vdc Line onto the test data sheet.

5.15.2 Repeat for the – 12 Vdc line.

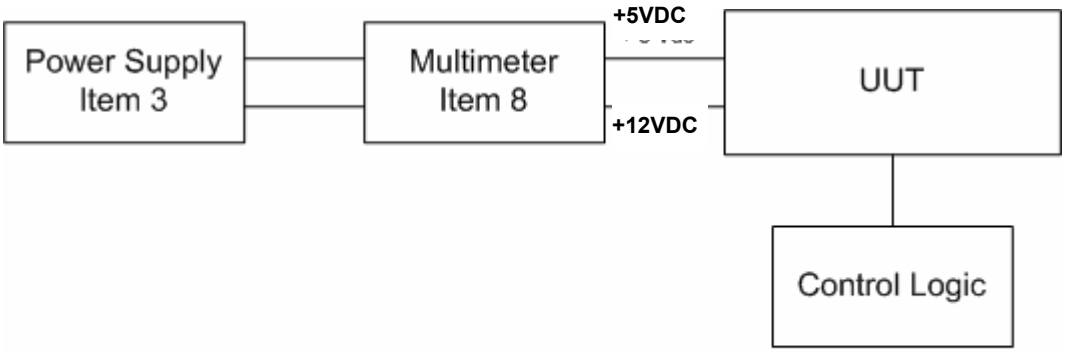

FIGURE VIII

6.0 INSERTION LOSS, VSWR, AND ISOLATION

6.1 Calibration of the Vector Network Analyzer (VNA). (For Insertion Loss, Isolation, and VSWR tests)

6.1.1 Connect the test equipment as in Figure IX. Set VNA with frequencies from 20.7GHz to 1.3 GHz. Set RF power level to + 5 dBm. Connect the open on Port 1 and short to Port 2. Press Cal button, then select full 2 port Cal and follow VNA instructions.

6.1.2 Save calibration to the registry.

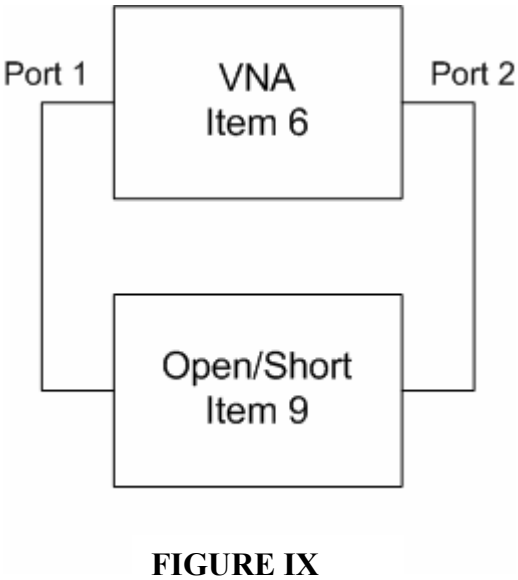

FIGURE IX

6.2 Measurement of the Unit Under Test (UUT).

6.2.1 Connect the test equipment and the UUT as in Figure X with common port (J1) as RF input and (J5) as RF output.

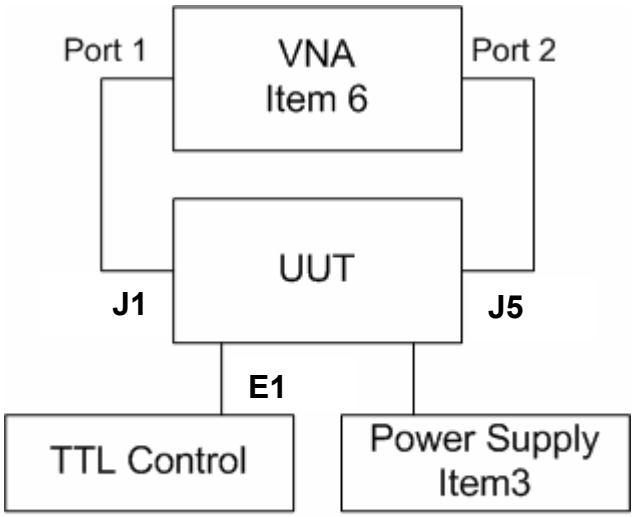

FIGURE X

6.2.2 Apply the TTL Logic Code to the UUT via the Table III.

6.2.3 INSERTION LOSS (SELECTED PATH GAIN)/LOSS FLATNESS

6.2.3.1 Observe and record onto the Test Data Sheet the worst case insertion loss (S21) displayed on the VNA.

6.2.3.2 Observe and record onto the Test Data Sheet the insertion loss flatness for any 50MHz Band (S21) displayed on the VNA.

6.2.3.3 Repeat for path J2 to J5.

6.2.3.4 Repeat for path J3 to J5.

6.2.3.5 Repeat for path J4 to J5.

6.2.4 VSWR

6.2.4.1 Observe and record the worst case input (S11) VSWR, displayed on the VNA, onto the Test Data Sheet for the J1 to J5 path,

6.2.4.2 Repeat for path J2 to J5.

6.2.4.3 Repeat for path J3 to J5.

6.2.4.4 Repeat for path J4 to J5.

6.2.5 ISOLATION

6.2.5.1 Set VNA to observe S21, press display to memory then press data/memory button to calibrate out the insertion loss.

6.2.5.2 Apply proper logic to the UUT to have no RF thru path J1 to J5.

6.2.5.3 Observe and record onto the test data sheet the worst case isolation displayed on the VNA.

6.2.5.4 Repeat for path J2 to J5.

6.2.5.5 Repeat for path J3 to J5.

6.2.5.6 Repeat for path J4 to J5.

Model No: SWN-RRA-2DR-LSI
Options: NG, DB
Lot Acceptance Test Data Sheet 1 of 1

JOB: _____ CUSTOMER: _____

S/N: _____ TESTED BY: _____ DATE: _____

QA APPROVAL: _____ DATE: _____

Para.	Parameter	Requirement	Tolerance	Measured Value	Pass/Fail
4.1.1.3	Switching Time				
	ON to OFF	25ns	Max.	ns	
	OFF to ON	25ns	Max.	ns	
4.1.1.4	Rise/Fall Time				
	Rise	2.5ns	Max.	ns	
	Fall	2.5ns	Max.	ns	
4.2.2	Video Feedthru	Duration of 30ns from 50% point			
	J5-J1	-70dBm	Max.	dBm	
	J5-J2	-70dBm	Max.	dBm	
	J5-J3	-70dBm	Max.	dBm	
	J5-J4	-70dBm	Max.	dBm	
4.2.3	Video Feedthru	Duration of 25ns from 50% point			
	J5-J1	-60dBm	Max.	dBm	
	J5-J2	-60dBm	Max.	dBm	
	J5-J3	-60dBm	Max.	dBm	
	J5-J4	-60dBm	Max.	dBm	
	Power Supply Sequencing		Pass/Fail		
	Power Supply Coupling		Pass/Fail		
	Response Time				

Model No: SWN-RRA-2DR-LSI
Options: NG, DB
Acceptance Test Data Sheet 1 of 2

JOB: _____ CUSTOMER: _____

S/N: _____ TESTED BY: _____ DATE: _____

TEMP:_____ QA APPROVAL: _____ DATE: _____

Para.	Parameter	Requirement	Tolerance	Measured Value	Pass/Fail
5.1	Frequency Range				
		0.7 GHz to 1.3 GHz	Range	GHz	
5.2	Selected Path Gain				
	J5-J1	-2dB	±0.6dB	dB	
	J5-J2	-2dB	±0.6dB	dB	
	J5-J3	-2dB	±0.6dB	dB	
	J5-J4	-2dB	±0.6dB	dB	
5.3	Gain Deviation				
	J5-J1	-2dB	±0.6dB	dB	
	J5-J2	-2dB	±0.6dB	dB	
	J5-J3	-2dB	±0.6dB	dB	
	J5-J4	-2dB	±0.6dB	dB	
5.4	Noise Figure	Test at all Temperatures			
	J5-J1	13 dB	Max	dB	
	J5-J2	13 dB	Max	dB	
	J5-J3	13 dB	Max	dB	
	J5-J4	13 dB	Max	dB	
5.5	Maximum RF Input Signal				
		Must Operate at +25dBm CW	Pass/Fail		
		Must Operate at +25dBm Pulsed	Pass/Fail		
5.6	Input 1 dB Compression Point	Test at all Temperatures			
		6 dB	Min.	dB	
5.7.1.1	Harmonics				
	3 dBm RF Input	-20 dBc	Max.	dBc	
	-20 dBm RF Input	-65 dBc	Max.	dBc	

Model No: SWN-RRA-2DR-LSI
Options: NG, DB
Acceptance Test Data Sheet 2 of 2

JOB: _____ CUSTOMER: _____

S/N: _____ TESTED BY: _____ DATE: _____

TEMP:_____ QA APPROVAL: _____ DATE: _____

5.7.1.2	Spurious Signals				
	3 dBm RF Input	-60 dBc	Max.	dBc	
	-20 dBm RF Input	-65 dBc	Max.	dBc	
5.8	RF Isolation				
	J5-J1	-65 dB	Min.		
	J5-J2	-65 dB	Min.		
	J5-J3	-65 dB	Min.		
	J5-J4	-65 dB	Min.		
5.9	Insertion Phase Variation	Test at all Temperatures			
	J5-J1	For any 50MHz segment	±1.5°	°	
	J5-J2	For any 50MHz segment	±1.5°	°	
	J5-J3	For any 50MHz segment	±1.5°	°	
	J5-J4	For any 50MHz segment	±1.5°	°	
5.10	Insertion Gain Variation	Test at all Temperatures			
	J5-J1	For any 50MHz segment	±0.3dB	dB	
	J5-J2	For any 50MHz segment	±0.3dB	dB	
	J5-J3	For any 50MHz segment	±0.3dB	dB	
	J5-J4	For any 50MHz segment	±0.3dB	dB	
5.11	Input VSWR	Nominal Impedance 50 OHMS			
	J5-J1	1.4:1	Max.		
	J5-J2	1.4:1	Max.		
	J5-J3	1.4:1	Max.		
	J5-J4	1.4:1	Max.		
5.11	Output VSWR	Nominal Impedance 50 OHMS			
	J5-J1	1.6:1	Max.		
	J5-J2	1.6:1	Max.		
	J5-J3	1.6:1	Max.		
	J5-J4	1.6:1	Max.		
5.12.1	Switch Control				

Model No: SWN-RRA-2DR-LSI
Options: NG, DB
Acceptance Test Data Sheet 2 of 2

JOB: _____ **CUSTOMER:** _____

S/N: _____ **TESTED BY:** _____ **DATE:** _____

TEMP:_____ **QA APPROVAL:** _____ **DATE:** _____

	Characteristics Logic "1"				
	J5-J1				
	J5-J2				
	J5-J3				
	J5-J4				
5.12.2	**Switch Control Characteristics Logic "0"**				
	J5-J1				
	J5-J2				
	J5-J3				
	J5-J4				
5.13	**Control Lines**		**Pass/Fail**		
5.14	**DC Block**		**Pass/Fail**		
5.15	**DC Power Requirements**				
	+5VDC	**320 mA**	**Max.**		
	-12 VDC	**50 mA**	**Max.**		